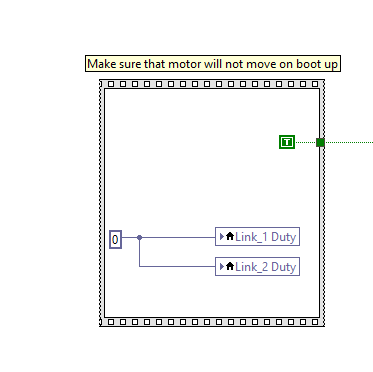
MyPAM MyRIO FPGA Documentation

The FPGA consists of a number of parallel loops. First, there is some simple initialisation, as shown by point 1:

1. Ensure that motors do not move on bootup by writing motor demand = 0

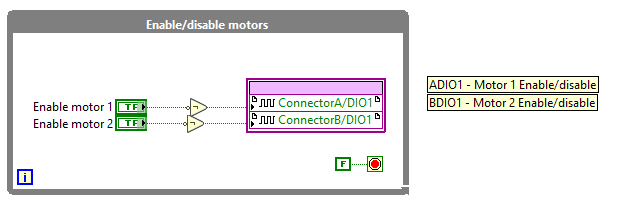


**Inputs**: None.

**Outputs**: Link\_1 Duty and Link\_2 Duty set to 0.

Following this initialisation, parallel loops. A loop reads enable/disable motors from the RT, and writes to digital lines which enable/disable the relays in the Hardware.

1. Read enable/disable motors, write to digital lines. Note, the signal is inverted because it was performing opposite as intended otherwise.



**Inputs**: Enable motor 1 (from RT), Enable motor 2 (from RT).

**Outputs**: ADIO1 (enable/disable relay), BDIO1 (enable/disable relay).